

Fig. 2 (a) Y0 (b) ER (c) VMI (d) MT1 (e) LU1

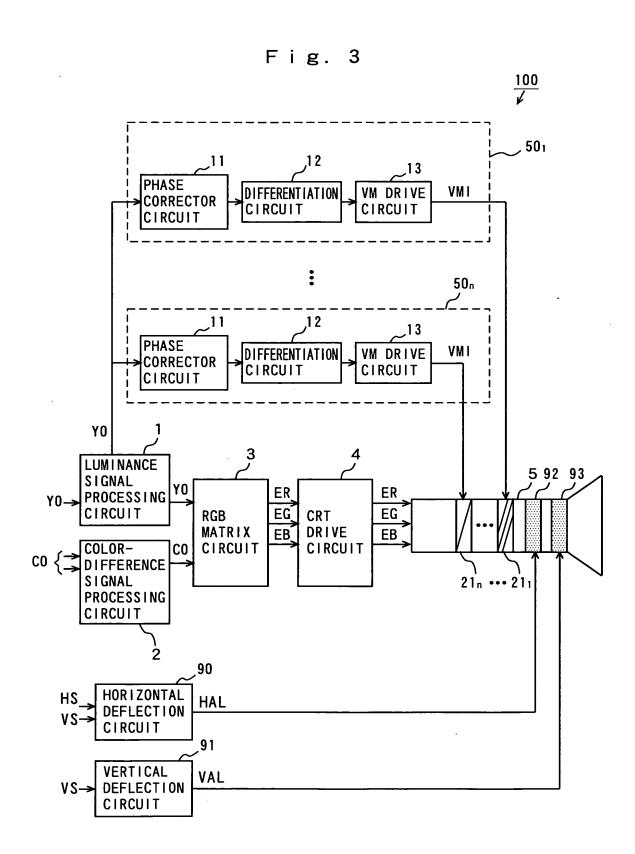


Fig. 4 100 50₁ **PHASE** 1 MV VM DRIVE CORRECTOR CIRCUIT CIRCUIT CIRCUIT 50_n PHASE VM DRIVE VMI DIFFERENTIATION CORRECTOR CIRCUIT CIRCUIT CIRCUIT Y0 LUMINANCE 5 92 93 SIGNAL YO PROCESSING Y0 ER ER CIRCUIT EG EG RGB **CRT** DRIVE MATRIX ΕB EB COLOR-DIFFERENCE CIRCUIT CIRCUIT C0 SIGNAL 21n --- 211 **PROCESSING** CIRCUIT 90 HORIZONTAL HAL **DEFLECTION** CIRCUIT 91 **VERTICAL** VAL DEFLECTION CIRCUIT VS->

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Fig. 5 100 50₁ PHASE VM DRIVE VMI CORRECTOR CIRCUIT CIRCUIT CIRCUIT 50n PHASE VM DRIVE VMI DIFFERENTIATION CORRECTOR CIRCUIT CIRCUIT CIRCUIT **Y0** 3 LUMINANCE 5 92 93 SIGNAL ER ER YO PROCESSING CIRCUIT EG EG RGB CRT MATRIX DRIVE ΕB ΕB COLOR-DIFFERENCE CIRCUIT CIRCUIT CO SIGNAL 21n --- 211 **PROCESSING** CIRCUIT 90 HORIZONTAL HS HAL **DEFLECTION** VS→ CIRCUIT 91 VERTICAL VAL DEFLECTION CIRCUIT VS->

Fig. 6

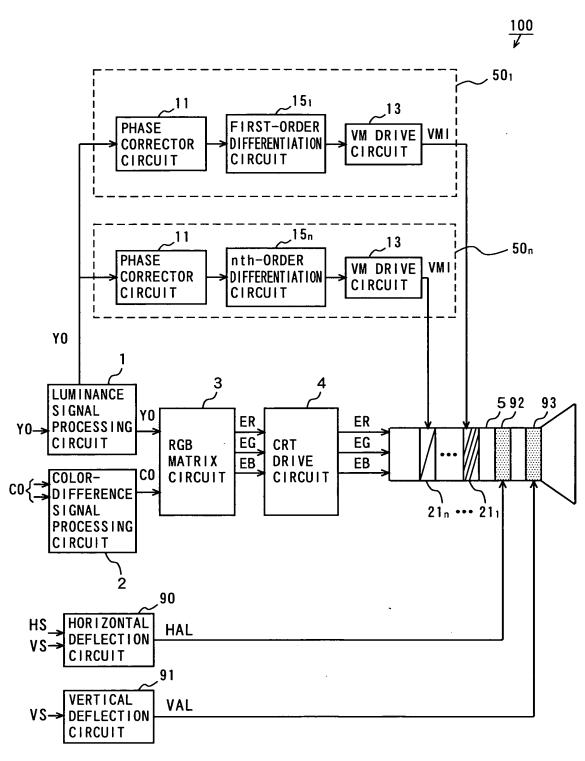


Fig. 7

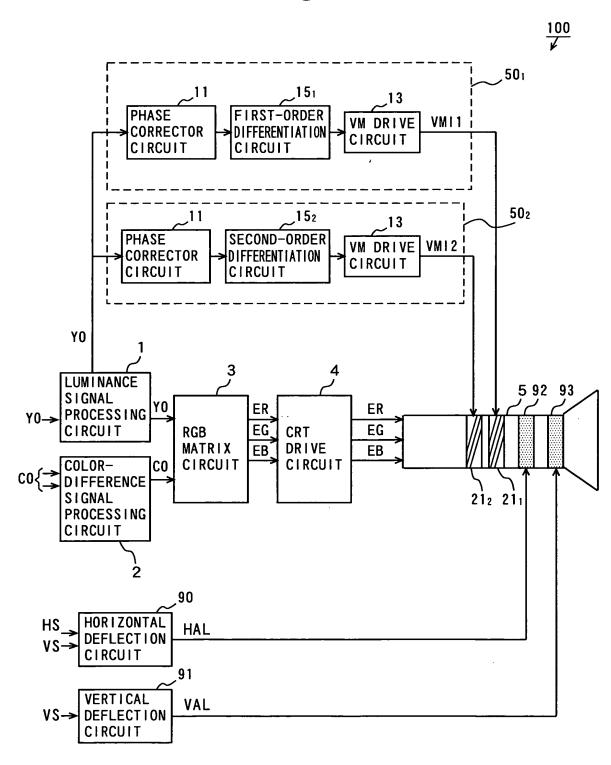


Fig. 8

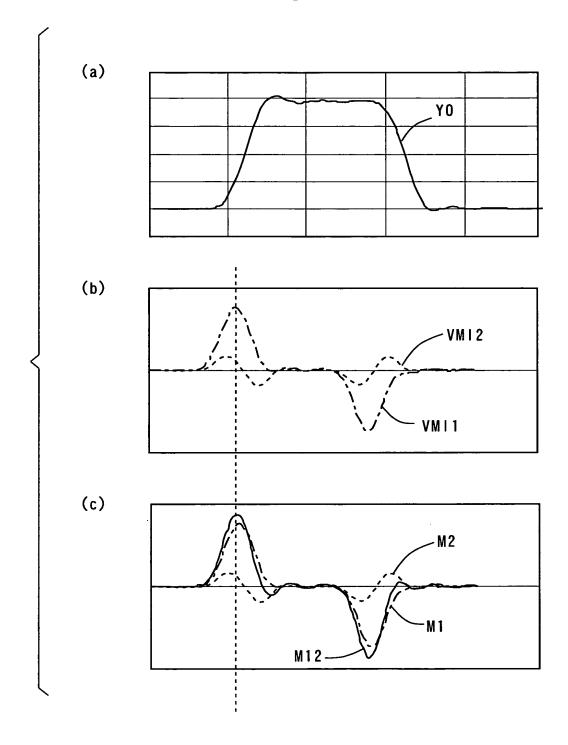


Fig. 9

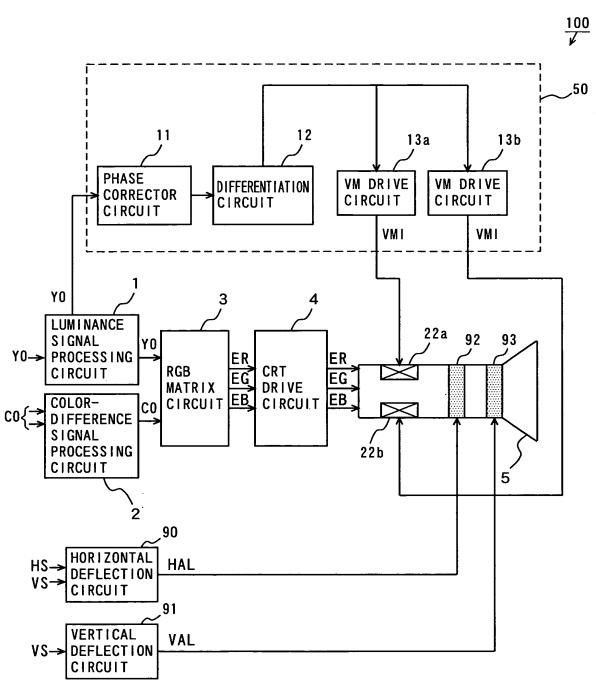


Fig. 10

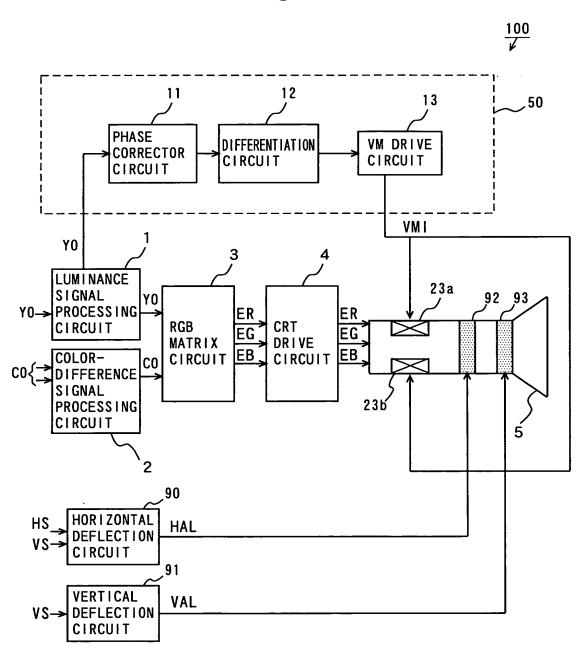


Fig. 11

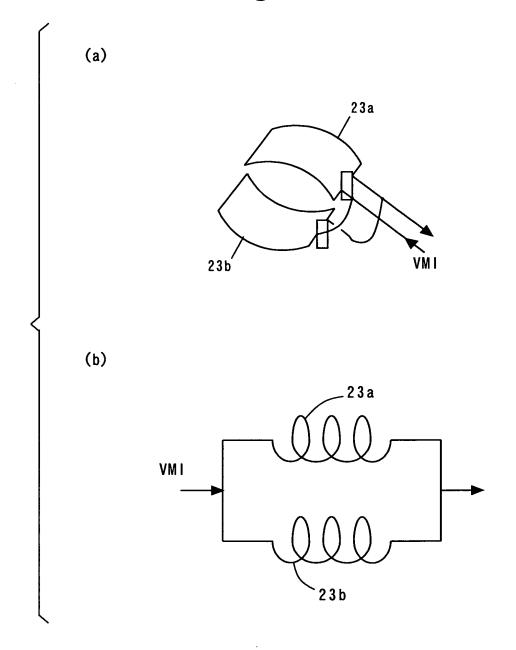


Fig. 12 PRIOR ART

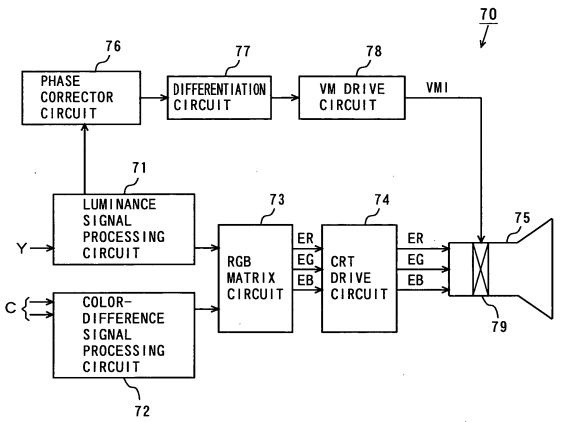
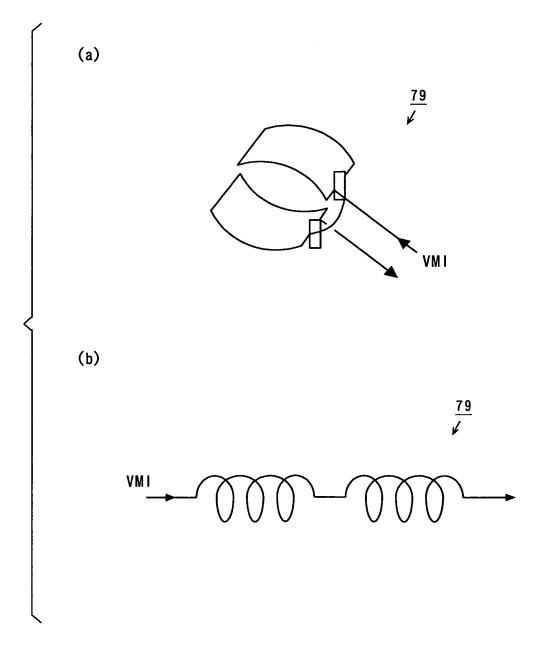


Fig. 13 PRIOR ART



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Fig. 14 PRIOR ART (a) Y (b) ER (c) VMI (d) MT (e) LU